



JRW
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Paul A. Farrar

Serial No.: 10/788,991

Filed: February 27, 2004

For: SURFACE BARRIERS FOR COPPER
AND SILVER INTERCONNECTS
PRODUCED BY A DAMASCENE
PROCESS

Confirmation No.: 6858

Examiner: G. Gurley

Group Art Unit: 2812

Attorney Docket No.: 2269-5570.1US
(02-1122.01/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

September 28, 2005

Date

Signature

Joseph A. Walkowski
Name (Type/Print)

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO/SB/08 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

10/03/2005 SDENB0B1 00000020 10788991

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In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicant herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

Other Documents

ANDRICACOS, Panos C., "Copper On-Chip Interconnections", The Electrochemical Society Interface, Spring 1999, pp. 32-37, Vol. 8, No. 1.

BRAUD et al., "Ultra Thin Diffusion Barriers for Cu Interconnections at the Gigabit Generation and Beyond", VMIC Conference, June 1996, pp. 174-179, 1996 ISMIC - 106/96/0174(c).

de FELIPE et al., "Electrical Stability and Microstructural Evolution in Thin Films of High Conductivity Copper Alloys", IEEE, 1999, IITC 99/293-295.

DING et al., "Copper Barrier, Seed Layer and Planarization Technologies", VMIC Conference, June 1997, pp. 87-92, 1997 ISMIC - 107/97/0087(c).

GODEBEY et al., "Copper Diffusion in Organic Polymer Resists and Inter-Level Dielectrics", Thin Solid Films, 31 Oct. 1997, pp. 470-474, Vols. 308-309.

IIJIMA et al. "Structure and Electrical Properites of Amorphous W-Si-N Barrier Layer for Cu Interconnections", VMIC Conference, June 1996, pp. 168-173, 1996 ISMIC - 106/96/0168(c).

"International Conference on Metallurgical Coatings and Thin Films", Program and Abstracts, April 1997, pp. 309, 313.

"Improved Metallurgy for Wiring Very Large Scale Integrated Circuits", International Technology Disclosures, 25 Sept. 1986, 1 page, Vol. 4, No. 9.

LYMAN et al., "Metallography, Structures and Phase Diagrams", Metals Handbook, 8th Edition, date unknown, pp. 300-302, Vol. 8, Metals Park, Ohio.

MARCADAL et al., "OMCVD Copper Process for Dual Damascene Metallization", VMIC Conference, June 1997, pp. 93-98, 1997 ISMIC - 107/97/0093(c).

MURARKA et al., "Copper Interconnection Schemes: Elimination of the Need of Diffusion Barrier/Adhesion Promoter by the Use of Corrosion Resistant, Low Resistivity Doped Copper", SPIE, Jan 1994, ppg. 80-90, Vol. 2335.

RYU et al., "Barriers for Copper Interconnections", Solid State Technology, April 1999, pp. 1-6, Vol. 42, Issue 4, p53.

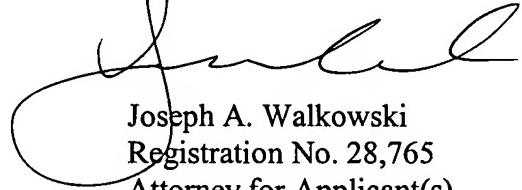
SAARIVIRTA, Matti J., "High Conductivity Copper-Rich Cu-Zr Alloys", Transactions of the Metallurgical Society of AIME, June 1960, pp. 431-437, Vol. 218, New York, NY.

Applicant offers to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed after the mailing date of the first Office Action on the merits.

The fee pursuant to 37 C.F.R. § 1.17(p) is enclosed.

Respectfully submitted,



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JAW/djp:slm

Enclosures: Form PTO/SB/08

Copy of documents cited

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PTO/SB/08B(10-01)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

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of

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Complete if Known

Application Number	10/788,991
Filing Date	February 27, 2004
First Named Inventor	Paul A. Farrar
Group Art Unit	2812
Examiner Name	L. Gurley
Attorney Docket Number	2269-5570 IIS (02-1122.01/IIS)

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		ANDRICACOS, Panos C., "Copper On-Chip Interconnections", The Electrochemical Society Interface, Spring 1999, pp. 32 37, Vol. 8, No. 1.	
		BRAUD et al., "Ultra Thin Diffusion Barriers for Cu Interconnections at the Gigabit Generation and Beyond", VMIC Conference, June 1996, pp. 174-179, 1996 ISMIC - 106/96/0174(c).	
		de FELIPE et al., "Electrical Stability and Microstructural Evolution in Thin Films of High Conductivity Copper Alloys", IEEE, 1999, IITC 99/293-295.	
		DING et al., "Copper Barrier, Seed Layer and Planarization Technologies", VMIC Conference, June 1997, pp. 87-92, 1997 ISMIC - 107/97/0087(c).	
		GODBEY et al., "Copper Diffusion in Organic Polymer Resists and Inter-Level Dielectrics", Thin Solid Films, 31 Oct. 1997, pp. 470-474, Vols. 308-309.	
		IIJIMA et al. "Structure and Electrical Properites of Amorphous W-Si-N Barrier Layer for Cu Interconnections", VMIC Conference, June 1996, pp. 168-173, 1996 ISMIC - 106/96/0168(c).	
		"International Conference on Metallurgical Coatings and Thin Films", Program and Abstracts, April 1997, pp. 309, 313.	
		"Improved Metallurgy for Wiring Very Large Scale Integrated Circuits", International Technology Disclosures, 25 Sept. 1986, 1 page, Vol. 4, No. 9.	
		LYMAN et al., "Metallography, Structures and Phase Diagrams", Metals Handbook, 8 th Edition, date unknown, pp. 300-302, Vol. 8, Metals Park, Ohio.	
		MARCADAL et al., "OMCVD Copper Process for Dual Damascene Metallization", VMIC Conference, June 1997, pp. 93-98, 1997 ISMIC - 107/97/0093(c).	
		MURARKA et al., "Copper Interconnection Schemes: Elimination of the Need of Diffusion Barrier/Adhesion Propoter by the Use of Corrosion Resistant, Low Resistivity Doped Copper", SPIE, Jan 1994, ppg. 80-90, Vol. 2335.	
		RYU et al., "Barriers for Copper Interconnections", Solid State Technology, April 1999, pp. 1-6, Vol. 42, Issue 4, p53..	
		SAARIVIRTA, Matti J., "High Conductivity Copper-Rich Cu-Zr Alloys", Transactions of the Metallurgical Society of AIME, June 1960, pp. 431-437, Vol. 218, New York, NY.	

Examiner Signature	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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